

REMARKS

Applicants request reconsideration of this application as amended.

Office Action Rejections Summary

Claims 1, 7, 19, 20, 21, 26 and 27 have been rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,198,751 of Dorsey et al. ("Dorsey").

Claim 13 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Dorsey.

Claims 2-6, 8-12 and 14-18 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Dorsey in view of U.S. Patent No. 6,181,694 of Pickett ("Pickett").

Claims 22-25 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Dorsey in view of U.S. Patent No. 6,747,995 of Brown et al. ("Brown").

Claim 22 has been objected to because of informalities.

Status of Claims

Claims 1-27 are pending in the application. Claim 22 has been amended to correct a typographical error. No claims have been added. No new matter has been added. No claims have been canceled.

The specification has been amended to correct minor matters of form. No new matter has been added.

Claim 22 has been objected to because of informalities. It is submitted that the amendment to claim 22 overcomes the objection.

Specification Amendment

In the Office Action dated 6/1/05, the Examiner stated that specification changes were needed on page 6, lines 10 and 11, to change the numeral character from "250" to "260". These changes were previously made in the response filed on December 20, 2004.

Applications are herewith submitting another change, amending "250" to "260", on page 6, line 15 to correct for a typographical error.

Claim Rejections

Claims 1, 7, 19, 20, 21, 26 and 27 have been rejected under 35 U.S.C. §102(e) as being anticipated by Dorsey. In response to Applicant's arguments that Dorsey discloses that controller 50 may be an ASIC, a PLD, or a general purpose CPU, the Office Action states: "It follows that from the above description that Dorsey description is related to prior art system and not to the controller." The Examiner's attention is also directed to column 5, lines 12-17 that clearly describe the controller 24 of Dorsey as being an ASIC or programmable logic device or that a general purposes processor could be used.

In response to Applicant's arguments, the Office Action also states:

In addition the function provided by the controller of Dorsey reads on that of the claimed DSP. Moreover, DSP are well known in the art, as shown by Brown reference (indicated above).

(Office Action, 6/1/05, page 9).

For argument sake, be that as it may, such is not a proper basis for establishing a prima facie rejection of the claims under 35 U.S.C. §102(e) as being anticipated by Dorsey. In particular, the assertion that "the function provided by the controller of Dorsey reads on that of the claimed DSP" is not a proper legal basis for rejecting the claims. It is submitted that the Examiner must show where Dorsey discloses a DSP in order to establish a prima facie rejection of the claims under 35 U.S.C. §102(e) as being anticipated by Dorsey. It is respectfully submitted that the Examiner has not done so and, moreover, it appears that the Examiner is in agreement that Dorsey does not disclose a DSP but, rather, a controller. The applicants have provided an argument and supporting documentation that establishes a DSP to be a different component than a controller. As previously argued, a DSP is a heterogeneous architecture from that of an ASIC, PLD or

general purpose CPU, as is well known in the art (See e.g., Different Device Types, techBites INTERActive, 2001 – submitted in an IDS filed with Applicant's previous Amendment and Response).

It is also submitted that the Examiner's reasoning that "DSP are well known in the art, as shown by Brown reference" is not pertinent to the current anticipation rejection under 35 U.S.C. §102(e) using only a single reference – that of Dorsey. Under an anticipation rejection under 35 U.S.C. §102(e), the Examiner must demonstrate where in the cited reference (i.e., Dorsey) the claim limitations of the present invention are disclosed. Moreover, should the Examiner issued an obvious rejection using the combination of Brown with Dorsey, the Examiner is respectfully reminded that he must identify a proper motivation within the references to make such a combination.

In response to Applicant's arguments, the Office Action also states:

Applicants also argue that the bus of claim 1 is not similar to the Dorsey's bus, because Dorsey bus is not a host port interface bus. **Examiner respectfully disagrees, the claimed "host port interface bus" is simply interpreted as "bus" since it doesn't provide any different functionality other than that provided by Dorsey's bus.** Examiner submit that the HPI buses are well established in the art, and they are used for interprocessors communications (inter-DSPs communications), However claim 1 recite one single DSP in connection to the (HPI) bus, it is within this context of a single DSP and a bus that Examiner interpreted the claim limitations.

(Office Action, 6/1/05, page 9)(emphasis added).

Applicants respectfully disagree with the Office Action's assertions and submit that the Office Action's interpretation of "host port interface bus" as simply a "bus" is inapposite. It is submitted that a host port interface (HPI) has a specific meaning that is well known to those of ordinary skill in the art as admitted by the Office Action and also seen, for example, by U.S. Patent No. 6,747,995 of Brown et al. cited by the Office Action. A HPI bus is a bus that is connected to a port of a host through which the host

can directly accesses the memory space of a connected processing device. In particular, an HPI bus supports both address and data busing.

In contrast to the HPI bus recited in claim 1, the bus disclosed in Dorsey [it is noted that the number "16" does not appear to be a reference numeral but, rather, refers to the number of bits of the bus] appears to be an instruction bus that does not include addressing. As can be seen by an inspection of Figure 5 of Dorsey, a separate address bus is connected between the address control 51b and the controller 50/opcode memory 51a. (See Dorsey, col. 8, lines 16-18; Figure 5). It is improper for the Office Action to interpret the bus of Dorsey as an HPI bus where there is no such disclosure in Dorsey.

Therefore, for at least the reasons provided above, it is submitted that claim 1 is patentable over Dorsey. For reasons similar to those given above with respect to claim 1, it is submitted that claims 7, 19, 20, 21, 26 and 27 are patentable over Dorsey.

Claim 13 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Dorsey. For reasons similar to those given above in regards to claim 1, it is submitted that Dorsey does not teach or suggest deliver a service program to a "digital signal processor" from an overlay memory over a "host port interface bus," as recited in claim 13. Therefore, claim 13 is patentable over Dorsey.

Claims 2-6, 8-12 and 14-18 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Dorsey in view of Pickett. Claims 2-6, 8-12 and 14-18 depend from and include the limitations of their respective independent claims 1, 7 and 13. It is submitted that Pickett fails to cure the deficiency noted above with respect to Dorsey. Therefore, it is submitted that claims 2-6, 8-12 and 14-18 are patentable over the cited references.

The Office Action must show a motivation within Dorsey as to why one of skill in the art, facing the problem confronting the inventor of Dorsey, would be motivated to make such a purported modification of Dorsey that creates the case of obviousness.

It is submitted that there is no motivation to combine the cited references in the manner purported by the Office Action. In particular, Dorsey teaches a multi-protocol translator that uses a microcoded, pipelined control unit 59. The translator is microcoded in order to maintain flexibility and permit new translations to be performed on existing structures and pipelined to reduce the delay from memory read latency. (Dorsey, col. 7, line 64 to col. 8, line 1; Figure 5). Accordingly, substantial reconstruction and redesign of the elements shown in the Dorsey would be required to use the line card of Brown proposed by the Office Action and, therefore, one of skill in the art would not be motivated to make the purported combination of Brown with Dorsey. See *In re Rattie*, 270 F.2d 810 (CCPA 1959); MPEP 2143.01. Moreover, Dorsey explicit teaches the use of its microcoded, pipelined control unit architecture to reduce delay and, therefore, one of skill in the art would not be motivated to modify the pipelined architecture of Dorsey's control unit in favor of the architecture of Brown because such a modification would seem to decrease the throughput of Dorsey, rather than increase the throughput as purported by the Office Action. Therefore, it is submitted that claim 22-25 are patentable over the combination of cited references.

In conclusion, applicants respectfully submit that in view of the arguments and amendments set forth herein, the applicable rejections and objections have been overcome.


If the Examiner believes a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact Daniel Ovanezian at (408) 720-8300.

If there are any additional charges, please charge our Deposit Account No. 02-2666.

Respectfully submitted,

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Dated: 11/1, 2005


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